

REMARKS/ARGUMENTS:

Minor changes are made to this specification. Claims 1-4, 8-10, 15, and 21-32 are amended. Support for the phrase "chiefly composed of components of the substrate" can be found at p. 14, line 24-p. 15, line 2 of Applicant's specification. Claims 1-4, 8-10, 15, and 21-32 are pending in the application. Reexamination and reconsideration of the application, as amended, are respectfully requested.

The present invention relates to method and apparatus for processing a substrate and a plate used therein, and more particularly to method and apparatus for processing a substrate that enable surface roughening on a silicon substrate used in a solar cell or the like, and a plate used therein. (Applicant's specification, at p. 1, lines 9-13).

CLAIM REJECTIONS UNDER 35 U.S.C. § 102:

Claims 8, 10, 15, 30, and 31 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Smith et al. (U.S. Patent No. 4,661,203).

Claims 1, 3, 4, 21, 23-25, 27-29, and 32 stand rejected under 35 U.S.C. § 102(b) as being anticipated by JP 63164433 (JP '433).

Claims 1, 3, 4, 21, 23-25, 27-29, and 32 stand rejected under 35 U.S.C. § 102(b) as being anticipated by JP 56076242 (JP '242).

CLAIM REJECTIONS UNDER 35 U.S.C. § 103:

Claims 2, 22, and 26 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over JP 56076242 (JP '242).

Claims 2, 22, and 26 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over JP 63164433 (JP '433).

Claims 8-10 and 30 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Imahashi (U.S. Patent No. 5,695,564).

The Applicant respectfully traverses the above rejections.

Claims 1, 8, 15, 21, and 25 are the independent claims.

(1) Independent claims 1, 8, 15, 21, and 25

All of the independent claims are directed to a method for producing a solar cell and include as a limitation of the method "placing a substrate for a solar cell." None of the cited references teach or suggest "placing a substrate for a solar cell." Furthermore, these claims are characterized by a process for forming textures on a substrate by using residues being chiefly composed of components of the substrate as an etching mask. The cited references similarly fail to teach or suggest such a process.

Independent claims 1, 8, and 15 comprise the steps of placing a plate whose open area ratio of the opening portions in the peripheral region is smaller than in the control region, and forming fine textures on a surface of the substrate by using residues that are chiefly composed of components of the substrate as a etching mask.

Independent claim 21 has the limitation that "a number of residues are formed by an etching of the substrate during an RF power applying, wherein the residues are trapped in a space between the substrate and the plate." Independent claim 25 has the limitation that "a number of residues are formed by an etching of the substrate during an RF power applying, wherein the residues are attached to the surface of the substrate."

JP '433 discloses an invention for improving the etching rate by using the electrode 6 which has a higher opening ratio in the central part than in the

peripheral part thereby leading out of the plasma is concentrated on the part to be etched (JP '433, ABSTRACT).

However, JP '433 is silent with respect to forming fine textures on a surface of the substrate by using residues being chiefly composed of components of the substrate as an etching mask.

JP '242 uses a porous middle electrode 5 (small holes are uniformly dispersed on a surface plane of the electrode 5). The role of the electrode 5 is to protect the substrate from bombardment of plasma and to enhance an etching rate to 5 to 10 times greater.

However, JP '242 is silent as to the limitation that "a number of residues are formed by an etching of the substrate during an RF power applying, wherein the residues are trapped in a space between the substrate and the plate" (claim 21) or "the residues are attached to the surface of the substrate" (claim 25).

The Office at p. 3 of the Office Action states that "etching products will inherently be trapped, with or without a plate being placed over the substrate being etched."

In response, Applicant respectfully submits that the present invention is placing a plate of the claimed structure to enhance formation of the residues and to form textures 2 in the surface of the substrate 1. In fact, the Applicant's specification at p. 13, lines 15-17 states that "it is difficult to form the textures 2 under condition that the etching residues will not be left on the surface of the silicon substrate 1.

However, JP '433 and JP '242 only reveal enhancing the etching rate by a porous plate, and both references are silent with respect to etching the substrate by using residues or components that are trapped in a space between the substrate and

the plate, or attached to the surface of the substrate. Thus, JP '433 and JP '242 fail to teach or suggest the present invention.

In contrast it is an aspect of the present invention that,

“Basically, silicon evaporates when it is etched, part of which, however, does not evaporate completely and molecules bond to one another, thereby being left as residues on the surfaces of the substrate 1. In other words, in the invention, when the surface of the silicon substrate 1 is roughened through the reactive ion etching method and a similar dry etching method, a rate at which etching residues, chiefly composed of etched silicon, re-attach to the surface of the silicon substrate 1 is accelerated, so that the textures 2 are formed on the surface of the silicon substrate 1 by using the residues as a micro-mask for etching.” (Applicant’s specification, at p. 12, line 23-p. 13, line 9).

(2) Independent claim 8

The Office cites Smith for teaching $h=2d$. However, Smith fails to teach or suggest trapping residues that are chiefly composed of components of the substrate between the plate and the substrate and forming a texture on the substrate by using the residues as an etching mask.

The Office further rejects claim 8 as being obvious over Imahashi. However, Imahashi reveals uniform dispersion of process gas through many holes on the baffle plate 95 (Imahashi, column 12, lines 19 - 22). The baffle plate 95 is disposed to cover the gas supply pipe 92 (Imahashi, Fig. 6). Consequently, Imahashi’s plate is not designed to cover the substrate as taught by the present invention.

In Imahashi’s plate, process gas is distributed from the many holes, so that compounds are not trapped between the substrate W and the upper electrode 91. Regardless of diameter of the holes of the plate, the effect of the present invention of

forming the compounds between the plate and the substrate cannot be obtained by the teachings of Imahashi.

(3) Independent claim 15

The Office states that Smith teaches “chamfered apertures”. However, Smith fails to teach or suggest the character of forming textures on the substrate by trapping residues that are chiefly composed of components of the substrate between the plate and the substrate, and forming textures on the surface of the substrate by use of the residues on an etching mask.

(4) Dependent claims 2, 9, 22 and 26

Dependent claims 2, 9, 22, and 26 require that “the plate is placed to be spaced apart from the surface of the substrate by 5 to 30 mm.” The Office maintains that based upon either JP ‘242 or JP ‘433, it would be obvious to optimize the spacing to achieve the desired results.

Applicant respectfully disagrees. It is effective to limit the spacing to 5 to 30 mm from the surface of the substrate to the plate. The Applicant’s specification at p. 14, line 21-p. 15, line 4 states,

“It is preferable to perform etching while the plate 13 and the silicon substrate 1 are held to be spaced apart by a predetermined distance D (see Fig. 5). Herein, P = 5 to 30 mm. When arranged in this manner, silicon compounds produced during etching can be trapped in a space between the silicon substrate 1 and the plate 13, which makes it easier for residues chiefly composed of silicon to be generated on the substrate 1. Hence, not only the generation of residues, but also the formation of the textures 2 can be promoted.”

Applicant respectfully submits that there is nothing in the cited references to teach or suggest that optimizing the spacing will achieve the results discussed above.

The significance of spacing 5 mm to 30 mm is understood from the specification which states,

“When the distance D between the plate 13 and the silicon substrate 1 is less than 5 mm, the opening portions 14 in the plate 13 are transferred as a pattern on the surface of the silicon substrate 1 when the textures 2 are formed, thereby leaving unevenness on the surface. Conversely, when the distance D is greater than 30 mm, the effect of generating the residues faster to promote formation of the textures 2 is reduced.” (Applicant’s specification p. 14, lines 4 - 11).

Consequently, the claimed spacing is effective to form residues.

However, in JP ‘433, the third electrode 6 is fixed approximately in the middle of the second electrode 5 and the object 7 to be etched. In JP ‘242, porous electrode plate 5 is placed approximately in the middle of the electrodes 3 and 4. Both JP ‘433 and JP ‘242 are silent with respect to the distance between the plate and the substrate. Presumably, neither reference is aware of enhancing residues between the plate and the substrate.

In contrast, the present invention is enhancing trapping of the residues between the plate and the substrate by limiting the distance between the plate and the substrate. This allows for fabricating a textured substrate in a simple manner.

In light of the foregoing, Applicant respectfully submits that the cited references could not have anticipated or rendered obvious claims 1-4, 8-10, 15, and 21-32, because the cited references either alone or in combination fail to teach or

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suggest each and every claim limitation. Withdrawal of these rejections is thus respectfully requested.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (310) 785-4600 to discuss the steps necessary for placing the application in condition for allowance.

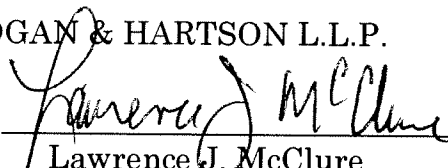
If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,

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